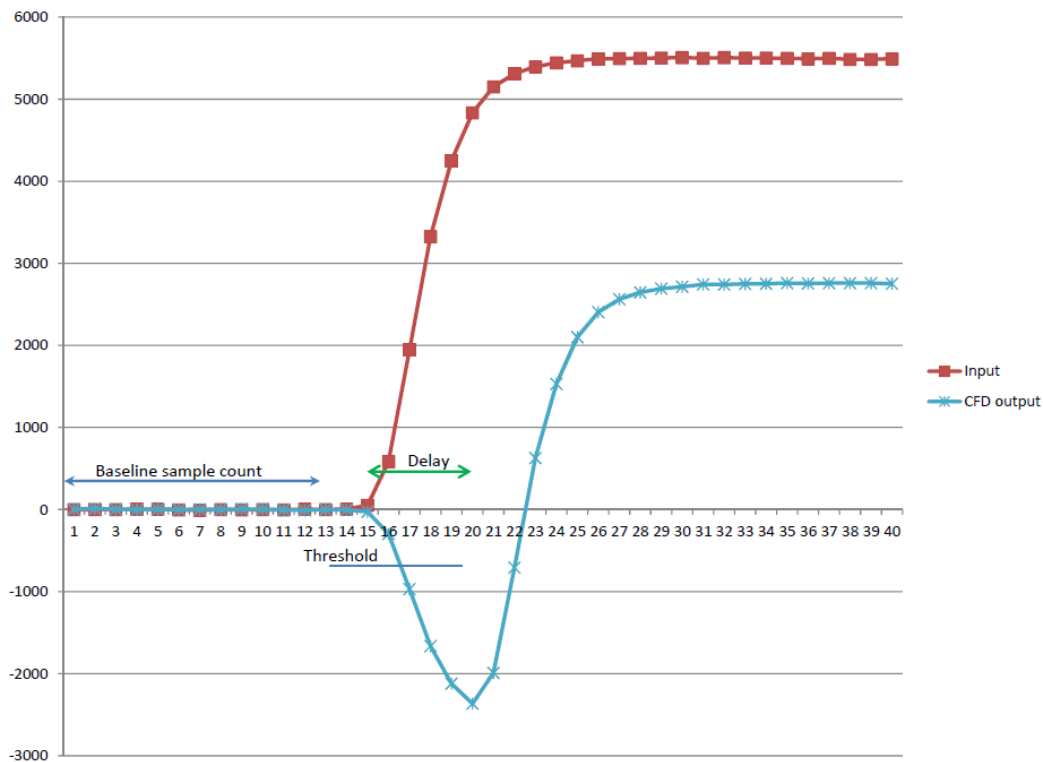# Considering the Vernier Timing unit in the FEE64

The object is to calculate the start time of a waveform, as a fraction of the 20nSec clock, using the zero crossing point of a CFD calculation.

This plot shows an input waveform and a 'cfd_output' as calculated by Excel.

Calculation

The Baseline is the average of the samples starting from T0 for the number of samples chosen by the user.

All samples are referenced to the Baseline before use.

CFD output is => (Delayed referenced input) – (Fraction of the referenced input)

At the point where the CFD output crosses 0 the two CFD output samples, one from before crossing and the other after crossing, are used to calculate the Vernier time.

The threshold is used to determine if the waveform will yield a Vernier.

The figure on the next page and the proof show how the Vernier is arrived at.
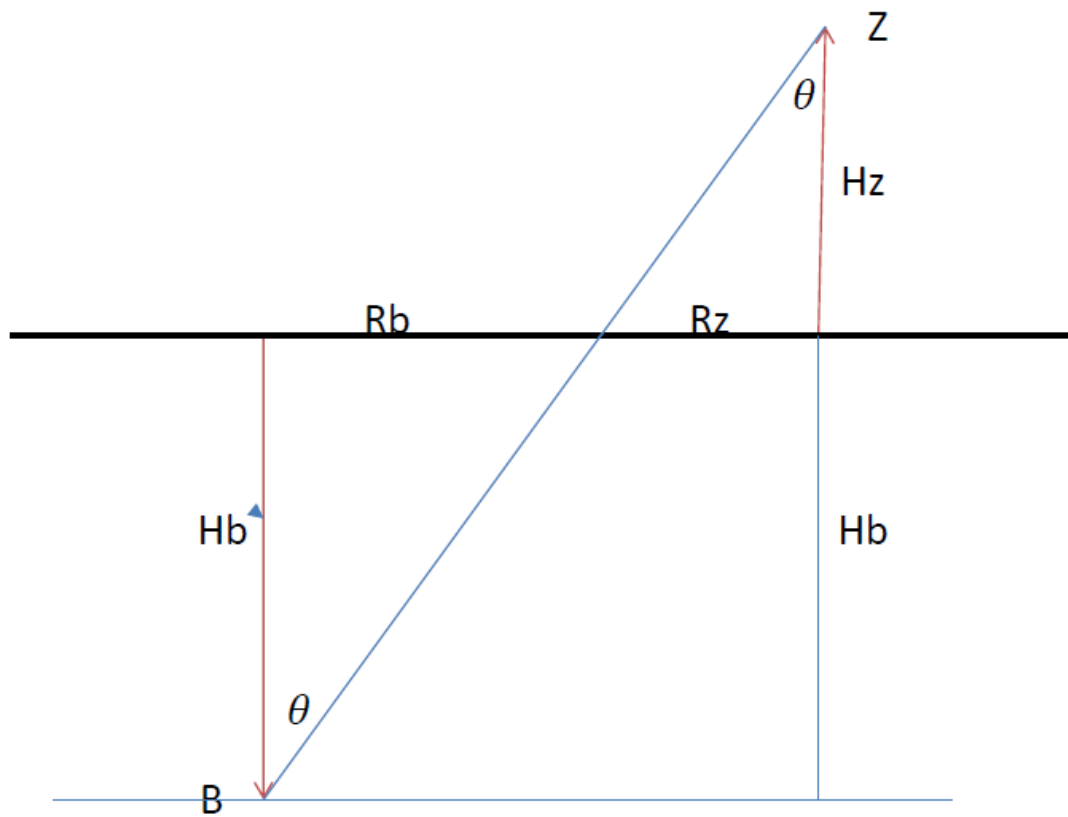
Consider the two triangles formed by the zero crossing. Assume the line joining the two points B(before Zero) and Z (after Zero) is straight.

θ is the angle the crossing line makes to the Vertical axis.

Hb is the sample value before the crossing and Hz is the sample after crossing.

Rb is the distance from the clock pulse to the crossing and Rz is the distance from the crossing to the next clock pulse.

The relationship between Rb and Rz is   Rb + Rz = 1 clock pulse = 20nS.

Also $Tan(\theta) = \dfrac{Rb}{Hb} = \dfrac{Rb+Rz}{Hb+Hz}$

However since Rz + Rb = 20nS

Time of crossing is $Rb = 20nS \times \dfrac{Hb}{Hb+Hz}$

Result:-

The Vernier value is attached to the end of the waveform data as it passes out from the VHDL to the memory of the Linux processor on the FEE64. The Data Acquisition software in the processor extracts it and creates a GREAT format ADC data item using the timestamp from the waveform. The 'Fail' bit is set to indicate it is a Vernier value.

The Vernier value is the 8 LSBs of the ADC data word. Bit 13 of the data part of the ADC data item is set if a Vernier has been calculated.

Tests:-

The FEE64 generates a SYNC pulse and outputs it on the FastTrigger signal to the MACB. The MACB output is connected to the External trigger input of a LeCroy pulser. The output of the LeCroy pulser is connected to the External Trigger input of a PB-5. The positive PB-5 signal is connected to the FADC input for ASIC2 channel 0. (NOTE:- *There is no ASIC in this test*)

The LeCroy pulser delay is stepped in 1nS increments. The Vernier spectrum is analysed using the "integrate" routine. The Vernier has a range of 0 to 255.

The spectrum shows the 20 peaks with 0 delay marked.
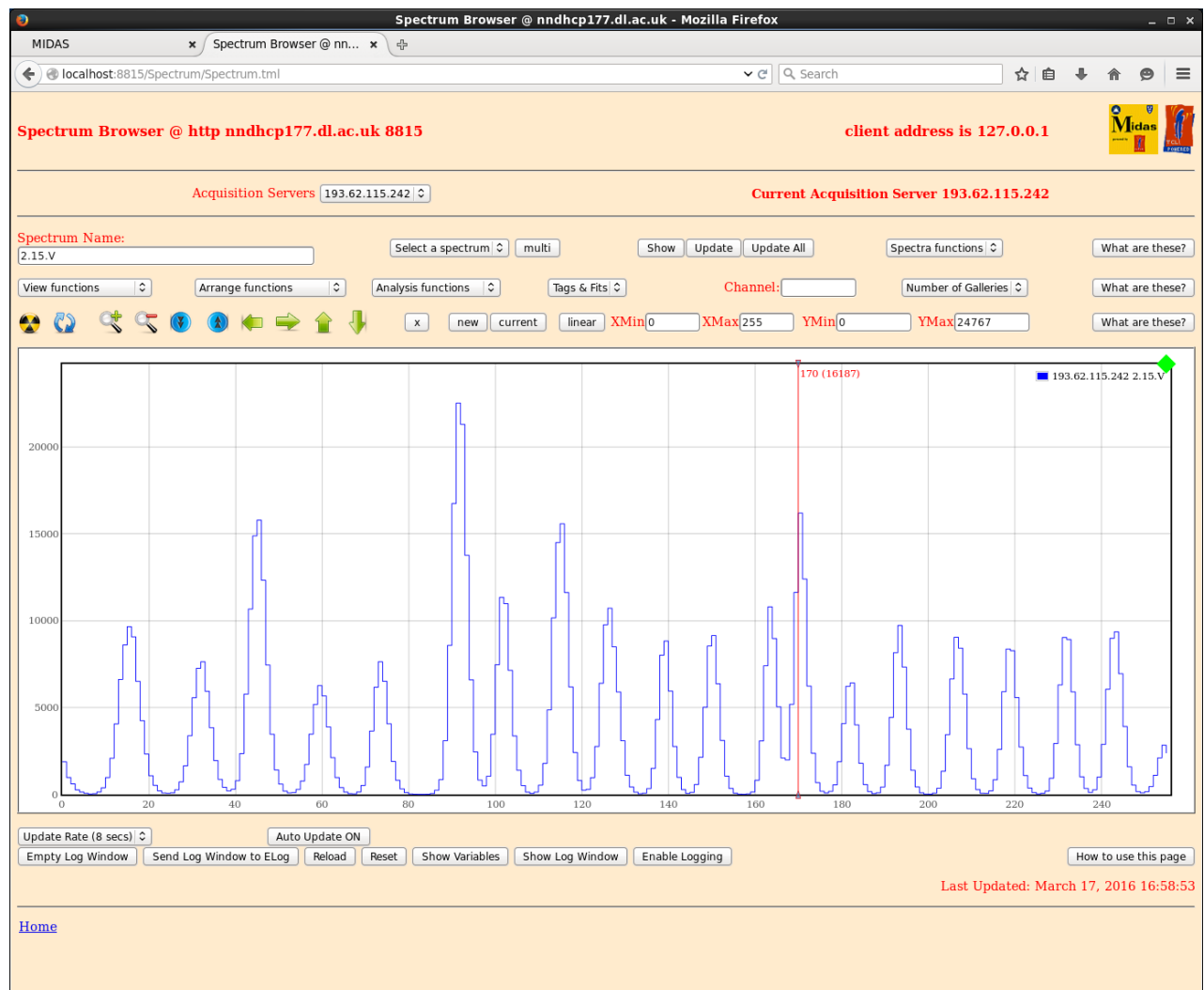
Setting up for operation

Threshold: +/- 0 to 8191.

> Set the value as an offset from the baseline. If the waveform is positive use a negative value etc.

Baseline sample count: 1 to 256 in steps of power of 2.

> The number of samples that are to be used to calculate the baseline. All the values are added together and then divided using a bit-shift. Hence only powers of 2 allowed. (1,2,4,8,16,32,64,128,256)

Fraction: 1 to 255.

> The multiplier for the CFD fraction. An eight bit number representing a fraction. So bit 7 is ½, Bit 6 is ¼ …… bit 0 is 1/256. Recommended value is 20% => 0.2 => 0x33 which is 19.9%.

Delay: 0 to 15.

> The number of samples (20ns clocks) to delay the input for the CFD calculation. The recommendation is 5 clocks.