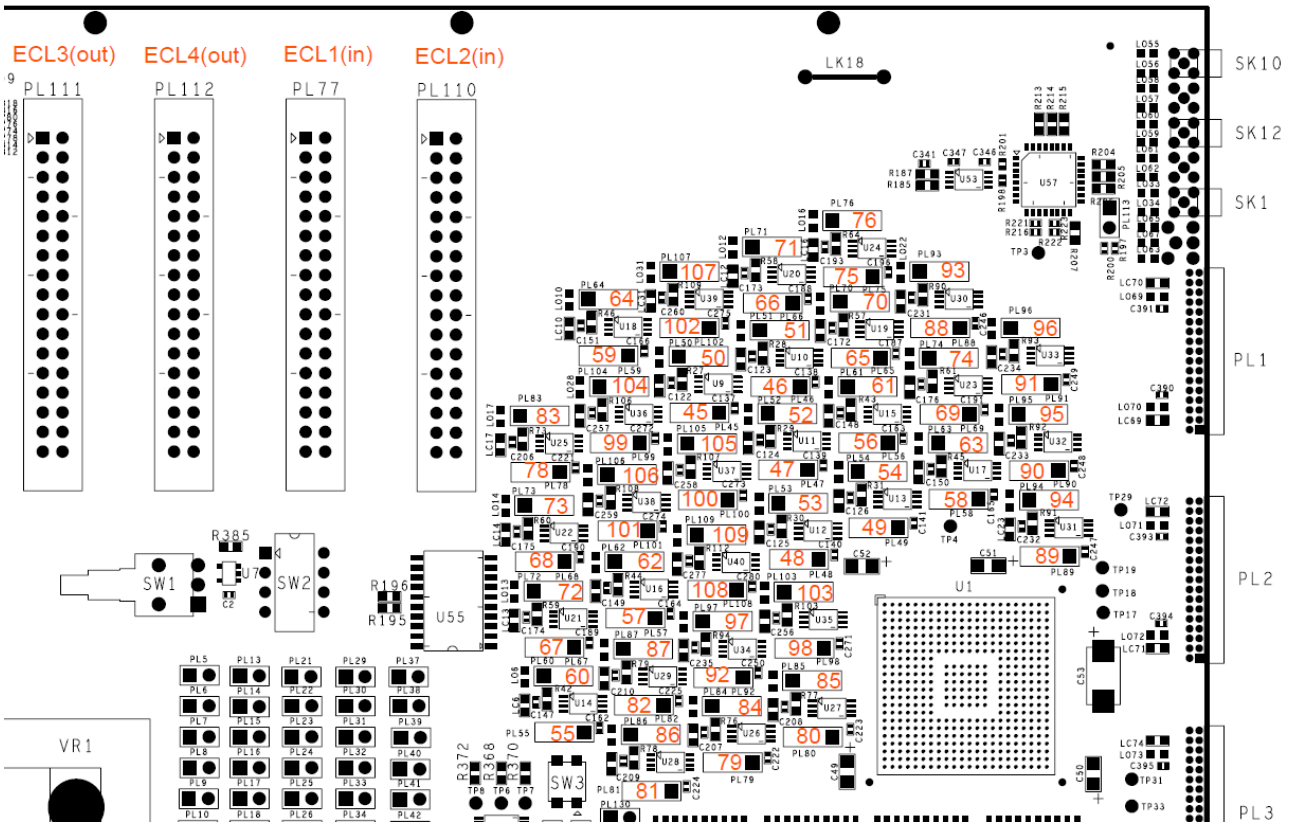
ECL Programming

ECL inputs can be set to either single ended or differential by jumpers (2 per input). For ECLline differential inputs as used by SAGE the jumpers must be set in the differential mode which means that **pins 2 and 3 must be connected together** on each jumper. Pin 1 is shown in the layouts as square; pins 2 and 3 are round although on the following diagram they have been removed to make jumper references more visible. Note that jumpers for the –ve ECL signal have pin 1 on the right and for the +ve ECL signal have pin 1 on the left (viewed from comp side, front panel on right).

Connector mates to PL77			**Connector mates to PL110**		
Signal	**-ve ECL jumper**	**+ve ECL jumper**	**Signal**	**-ve ECL jumper**	**+ve ECL jumper**
X1Vetoin1	PL45	PL50	X2Vetoin1	PL78	PL83
X1Vetoin2	PL46	PL51	X2Vetoin2	PL79	PL84
X1Vetoin3	PL47	PL52	X2Vetoin3	PL80	PL85
X1Vetoin4	PL48	PL53	X2Vetoin4	PL81	PL86
X1Vetoin5	PL49	PL54	X2Vetoin5	PL82	PL87
X1Vetoin6	PL55	PL60	X2Vetoin6	PL88	PL93
X1Vetoin7	PL56	PL61	X2Vetoin7	PL89	PL94
X1Vetoin8	PL57	PL62	X2Vetoin8	PL90	PL95
X1Vetoin9	PL58	PL63	X2Vetoin9	PL91	PL96
X1Vetoin10	PL59	PL64	X2Vetoin10	PL92	PL97
X1Vetoin11	PL65	PL70	X2Vetoin11	PL98	PL103
X1Vetoin12	PL66	PL71	X2Vetoin12	PL99	PL104
X1Vetoin13	PL67	PL72	X2Vetoin13	PL100	PL105
X1Vetoin14	PL68	PL73	X2Vetoin14	PL101	PL106
X1Vetoin15	PL69	PL74	X2Vetoin15	PL102	PL107
X1Vetoin16	PL75	PL76	X2Vetoin16	PL108	PL109



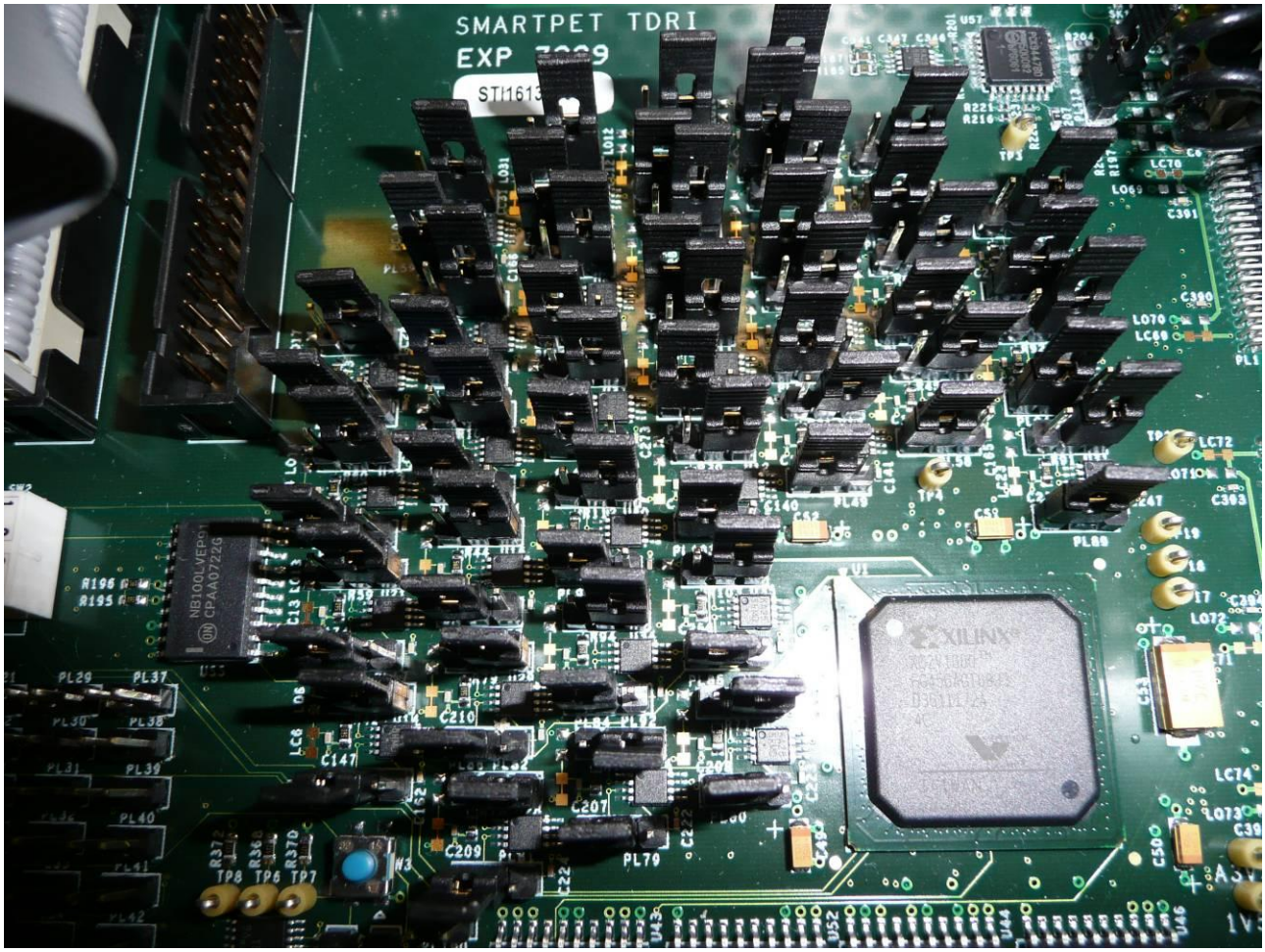


Photo of the ECL input jumpers with links set for differential mode (front panel on right of photo).

ECL outputs on PL111 and PL112 are differential ECL (no jumpers).

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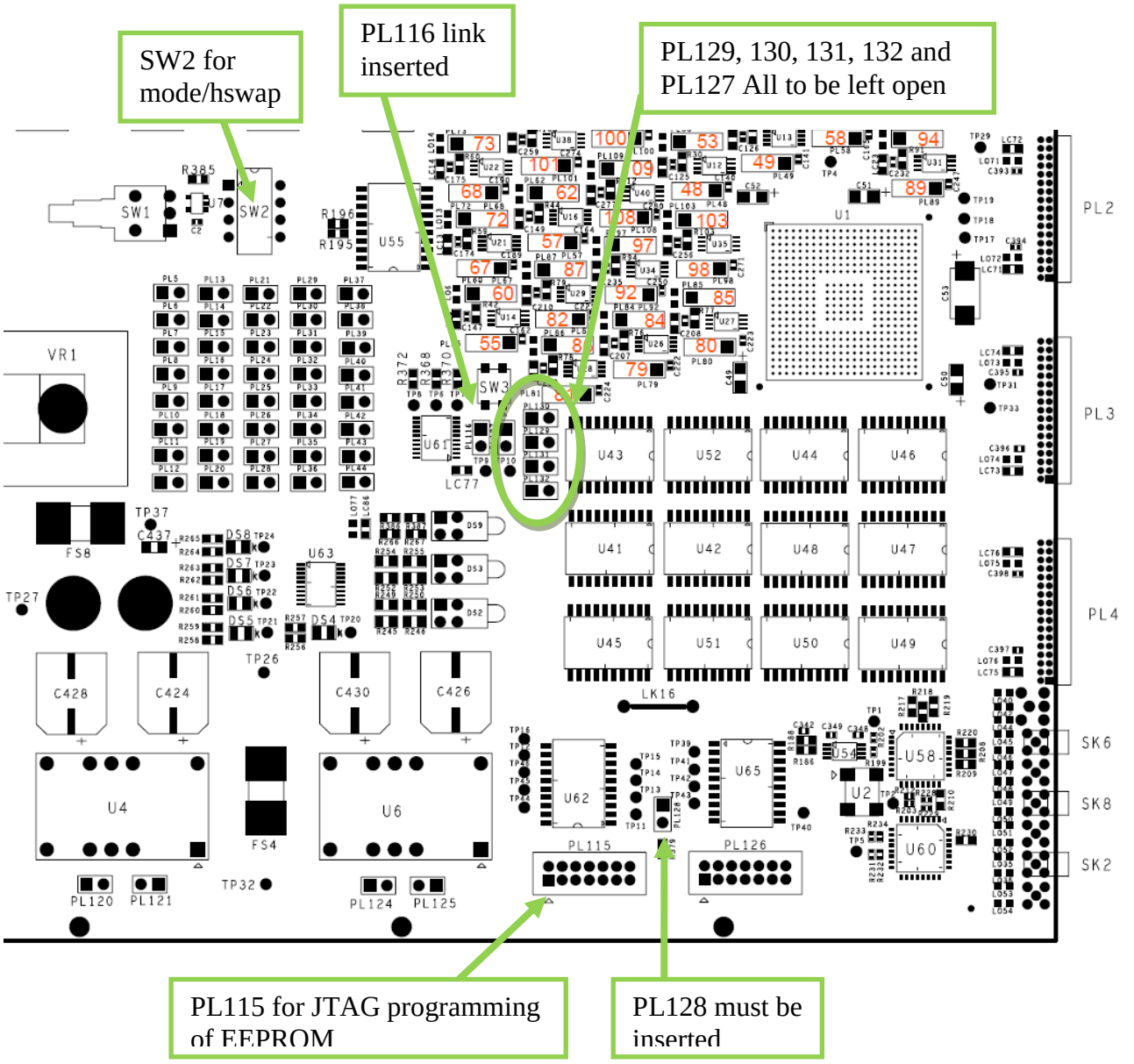
FPGA Programming

The FPGA program is loaded at power up (or reset using SW3) from an EEPROM. The EEPROM is programmed by a JTAG connection to **JTAG1 (PL115)**. It is necessary that link **PL128** is **inserted** to enable the 3 state driver which connects the JTAG input to the EEPROM. Link **PL116** must be **inserted.**

Other jumpers permit EEPROM programming from the XPORT- this is not yet supported so these jumpers must be set as follows so as not to interfere with JTAG programming. Links **PL129,130,131,132** must be **removed**. Link **PL127** must be **removed**

SW2 sets the FPGA mode lines (which control where the FPGA loads from) and HSWAP. The top switch of the 4 in SW2 (labelled 1) controls HSWAP. HSWAP =0 (switch on) puts pull ups on user i/o during configuration. Normally HSWAP = 1 (part 1 of SW2 set off).The other 3 switches in SW2 control the FPGA mode lines: 2 is M2, 3 is M1, 4 is M0. All are logic 0 when the switch is on. In normal operation the TDRI FPGA is programmed from the EEPROM using master serial mode (mode = 000) so **SW2 switches 2-4** should be **ON**.



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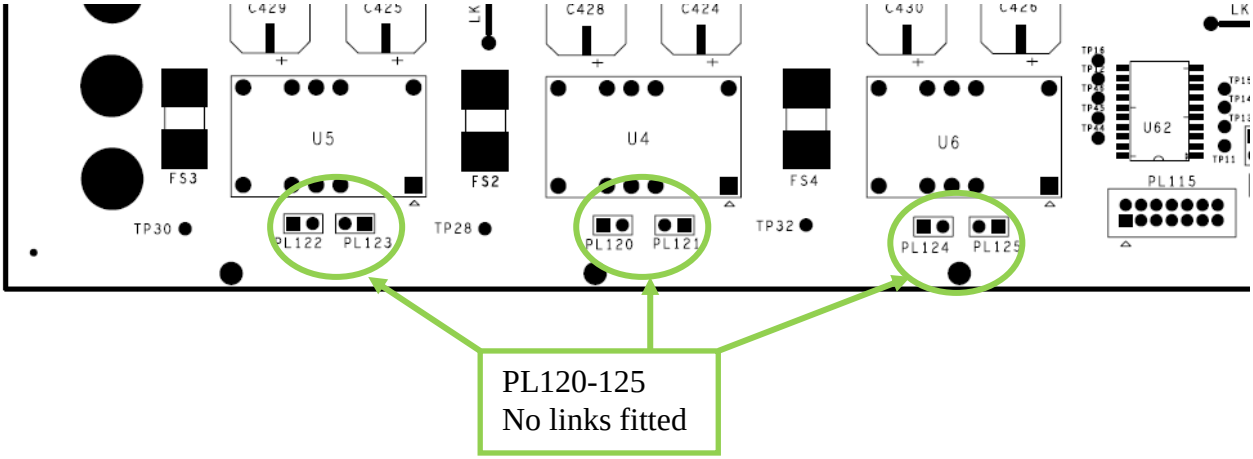
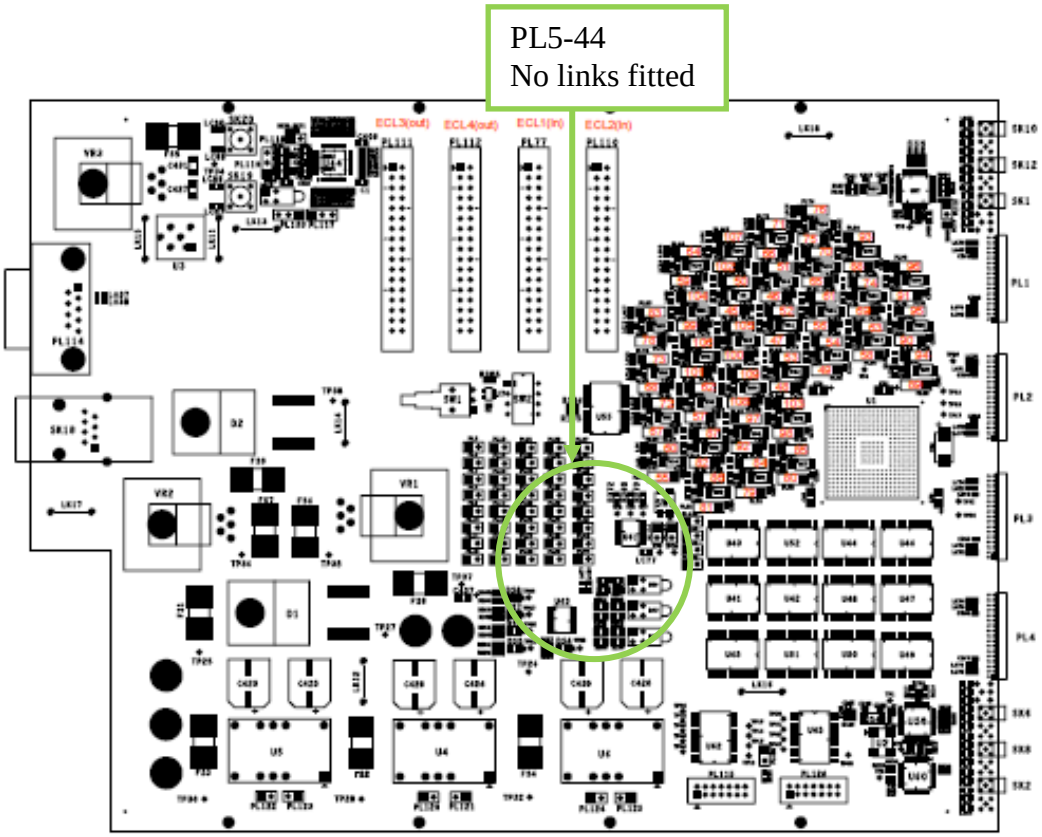
Other Jumpers

PL120, 121, 122, 123, 124, 125 are related to the power supplies. The power supply MU* and MD* pins can be connected to ground by these jumpers. MU* and MD* are Margin Up/Down controls to adjust outputs by +/-5%. In normal operation these links are **not fitted**.



PL5-44 all could be used to connect decouplers to Vref inputs to FPGA. **Links not fitted.**



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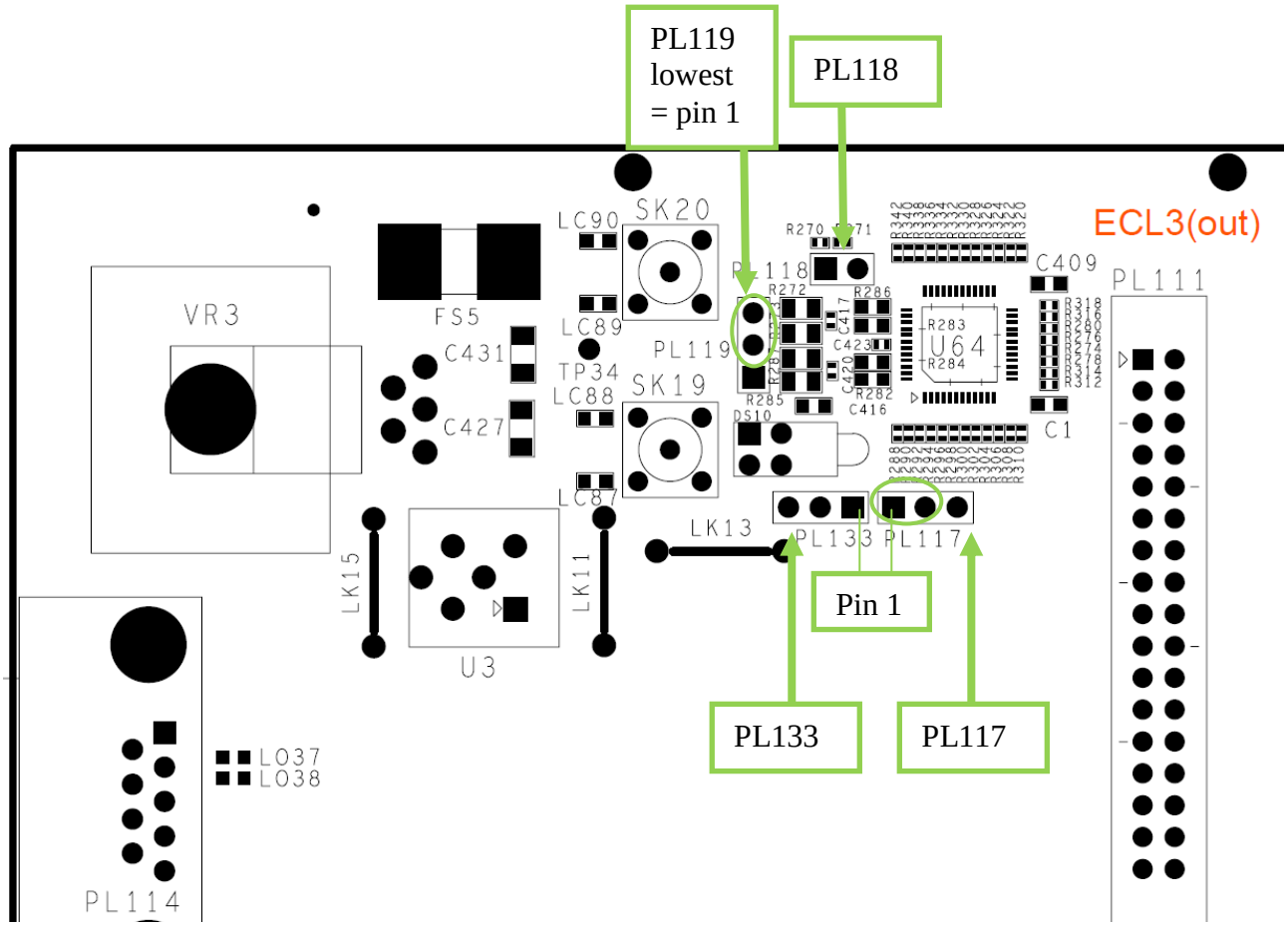
PL118 controls sleep of DAC- **leave open** (adding link connects sleep to 2V and sleeps DAC).

PL119 lowest pin is pin 1. Controls whether DAC GAINCTRL uses common or separate FS Adjust networks- on PCB there are 2 networks so TDRI needs the 2 network setting (GAINCTRL = AGND) which means connecting **pins 2 and 3**

PL133. **leave open** (no links)

PL117 leftmost pin is pin 1 (3v3), pin 2 is DAC MODE select , pin 3 is 0v. DAC MODE set to 1 = separate input control ports; 0 = interleaved commands from 1 input. TDRI uses separate inputs control ports so set to 1 by **connecting pins 1 and 2.**



The photo on the next page shows the area round the DAC jumpers (PL117, 118, 119, 133).

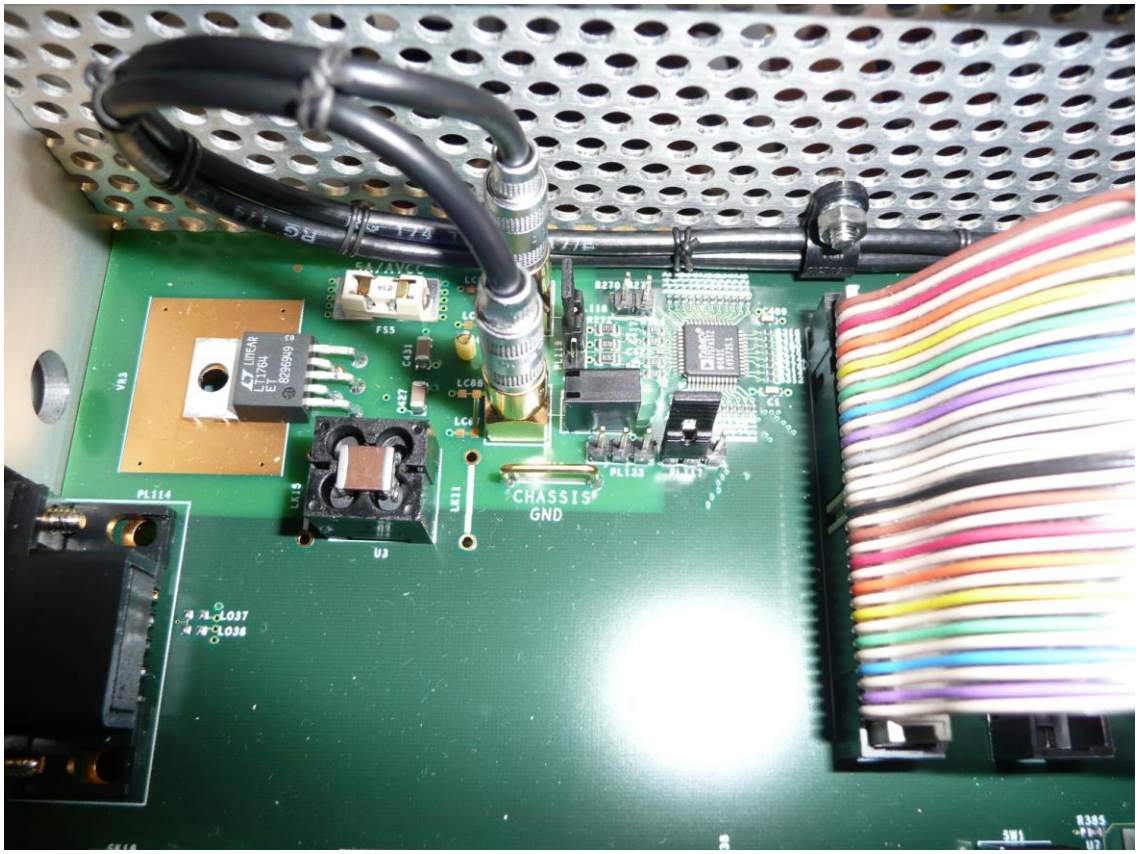
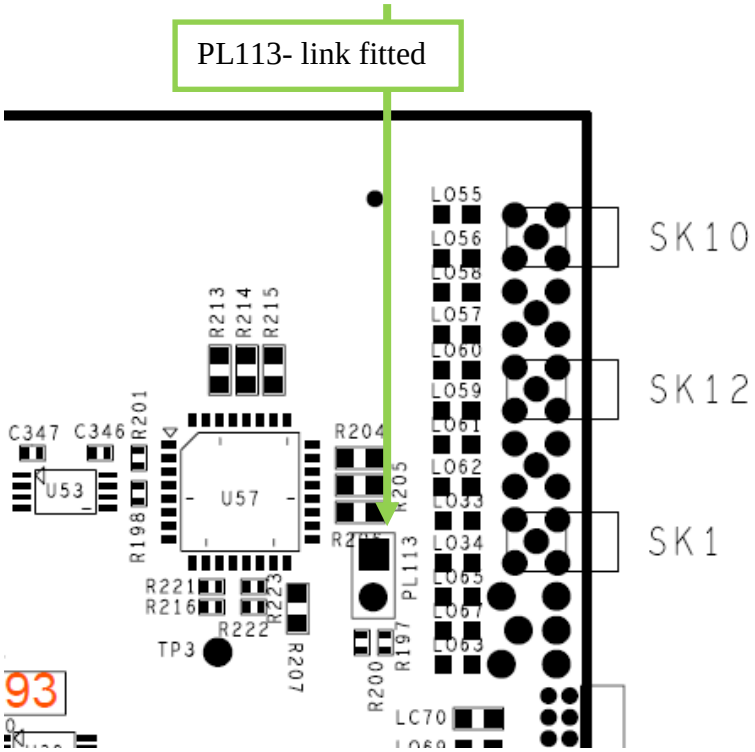


Photo of the jumpers controlling the DAC.

PL113 link inserted (Terminates incoming 100MHz front panel clock in 100ohms when inserted.)



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