**SmartPET Total Data Readout Interface (TDRI)**
**Implementation and Testing**
**Version: 1.0**
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## Introduction

TDRI distributes clock and control signals to the Smartpet VHS-ADC system. For a basic functional description see the following references.

Ref 1. Specification for smartpet Interface modules for Lyrtech VHS-ADC, draft 0.3 by I. Lazarus.
Ref 2. Smartpet: Specification for digitiser and processing tender, 1st Sep 2005 by I. Lazarus.

Fig1 below shows the top level block diagram of TDRI.

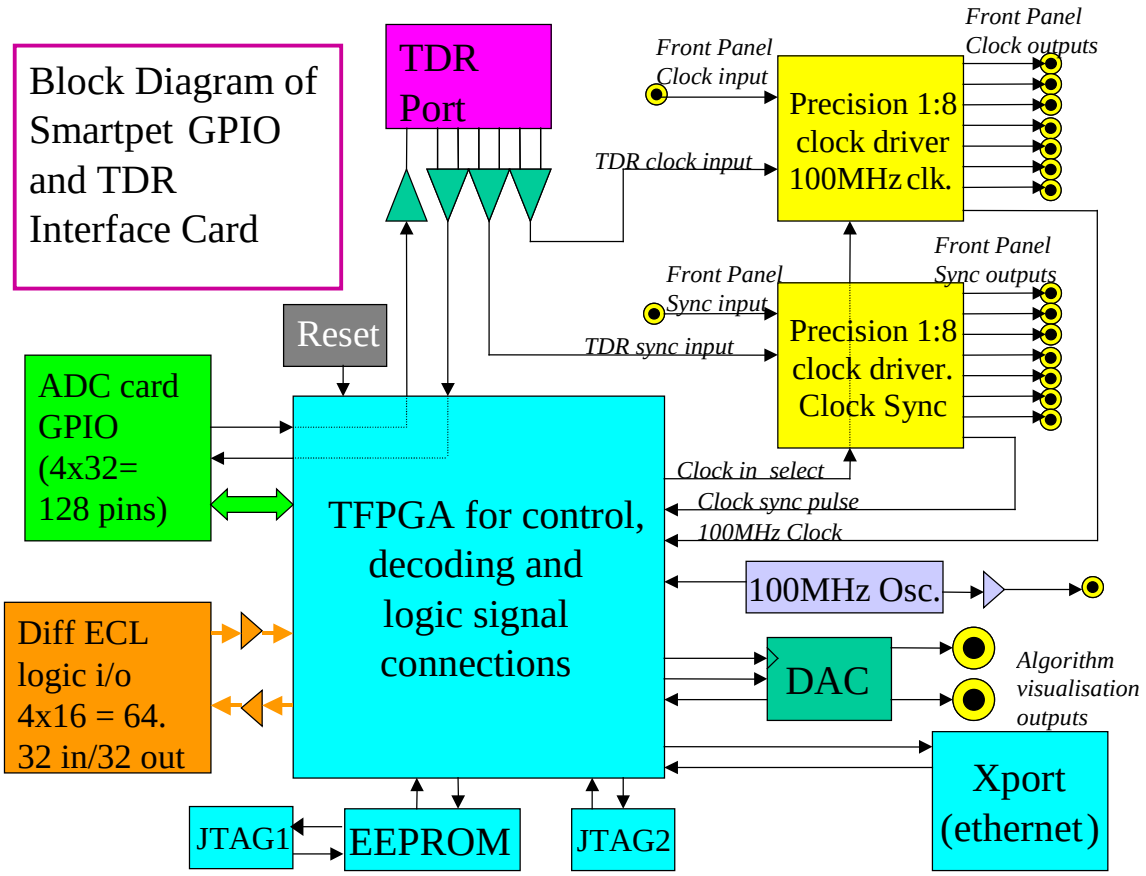


Fig1. Top level TDRI

At the heart of the TDRI is a Xilinx Virtex Π FPGA (TFPGA). The clock and control signals to the TFPGA come through the 'TDR Port'. TDRI fans out the Clock and Sync signals to the VHS-ADC cards. An optional test clock from '100 MHz Osc' is available on board TDRI.
Physics logic signals such as Veto and pattern, interfaces to the TFPGA via 'Diff ECL logic i/o'. The communication of the Physics logic signals and DAC Algorithm Visualisation data between the VHS-ADC and the TFPGA is via the 'ADC card GPIO' while the 'DAC' that is interfaced to the TFPGA allows the actual visualisation.
Computer control interface to the TFPGA is via Xport.
EEPROM and the TFPGA are on two separate JTAG chains.
Reset is connected to the TFPGA only and its function is under firmware control.
All digital signals on board TDRI are in LVTTL. However the logic standards at the connectors may differ and these are described under the appropriate sub sections below.

**TDR Port and 100 MHz Osc**

TDRI receives Clock and control signals from the VME Metronome unit through a nine pin D-Type connector at the TDR port. ERROR from the TFPGA is the only output signal on this connector.
Schematics Page (SchPg) 6 shows the circuits.
Nine pin D-Type connector is defined as follows.

| Pin Number | Function |
|---|---|
| 1 | 100MHz TDR CLOCK in NECL (H) |
| 2 | 0V |
| 3 | ERROR out NECL (H) |
| 4 | RESET in NECL (H) |
| 5 | SYNC in NECL (H) |
| 6 | 100MHz TDR CLOCK in NECL (L) |
| 7 | ERROR out NECL (L) |
| 8 | RESET in NECL (L) |
| 9 | SYNC in NECL (L) |

All the differential NECL input signals are level translated into LVTTL by 100EPT25. 100LVEP91 carries out the level translation of the ERROR output from LVTTL to NECL.

U57 has 7 off 50Ω series terminated LVTTL Clock fan-outs on the front panel MMCX sockets (SK10 – SK16). The source of the input clock to U57 is selectable by the FPGA signal XFPSEL
(NB. Commoned with Sync selection).

| XFPSEL | Source |
|---|---|
| 0 | External LVTTL Clock in through SK1 |
| 1 | TDR CLOCK in (Default if XFPSEL is in Tri-state) |

U58 has 7 off 50Ω series terminated LVTTL Sync fan-outs on the front panel MMCX sockets (SK3 – SK9). The source of the input Sync to U58 is selectable by the FPGA signal XFPSEL
(NB. Commoned with Clock selection).

| XFPSEL | Source |
|---|---|
| 0 | External LVTTL Sync in through SK2 |
| 1 | TDR Sync in (Default if XFPSEL is in Tri-state) |

All MMCX connectors are 50Ω.

**100 MHz Osc**:
U2 is a 100MHZ (+/- 50ppm) Crystal clock oscillator. SK17 has a continuously running 50Ω series terminated 100MHz LVTTL Crystal clock

**Testing:**
When using scope to probe outputs look for the quality and voltage levels of the waveforms.

Program XFPSEL = 0
Connect SK17 output to SK1 input. Using Scope, probe SK10 – SK16.
Connect SK17 output to SK2 input. Using Scope, probe SK3 – SK9.

Program XFPSEL = 1
Apply input signals to the TDR port.
Using Scope, probe SK10 – SK16.
Using Scope, probe SK3 – SK9.

## ADC Card GPIO

Four 34 way Samtec connectors, PL1 – PL4, shown in SchPg 7 provide this interface to allow direct connection between TFPGA and VHS-ADC FPGAs. Direction of the data flow is under firmware control.
The electrical signal standard on this interface is also under firmware control. VREF pins of the TFPGA can be connected to 1.5V (SchPg 1) for a wider choice of signalling standards.
**Caution:** TFPGA I/O operates on +3.3V supply. Voltages on the TFPGA I/O are compatible with only those listed in the Xilinx manual. Operating outside those recommendations can cause damage to FPGAs in general.

**Testing:**
Boundary Scan.
Custom Firmware.

**Diff ECL logic i/o**

There are 32 Physics Veto input signals and 32 output signals. All signals at the connectors are NECL.

**Inputs:**

SchPg 2–3 shows the inputs. Inputs can be 112Ω differential or 56Ω single ended NECL. Taking U9 (SchPg 2, top left) inputs as an example connect links PL45 and PL50 as follows to obtain the appropriate termination scheme.

For 112Ω differential termination:
PL45: Link 2A to 3A.
PL50: Link 2A to 3A.
Remaining pins not connected.

For 56Ω single ended termination:
PL45: Link 2A to 1A. (Connects inverted input to bias)
PL50: Link 2A to 1A. (Connects non-inverted input to 56Ω)
Remaining pins not connected.
**Caution:** Special single ended cable with no signals on the inverted inputs should be used to avoid damage to the NECL receivers, 100EPT25.

The LVTTL outputs from the receivers 100EPT25 are directly connected to the TFPGA.

**Testing Inputs:**

Boundary Scan.
Use Philips 7126 to generate input pattern. Design firmware to test inputs.

**Outputs:**

SchPg 4–5 shows the outputs. 100LVEP91 receive LVTTL signals from the TFPGA and outputs NECL differential signals to the 34 way IDC connector.

**Testing Outputs:**

Boundary Scan.
Use Philips 7126 to generate output pattern to the TDRI Inputs above. Design TFPGA firmware to pipeline the input pattern to the TDRI Outputs. Use Philips 7126 to capture and compare output and inputs patterns and generate an error count if any.

**Xport**

This is (SchPg 7, SK18) the Ethernet interface to the TFPGA. Signalling between Xport and TFPGA is to RS 232 standard in LVTTL.

**Testing:**

Boundary Scan.
Custom Firmware.

## DAC

The two-channelled DAC is shown in SchPg 9. DAC receives Algorithm Visualisation data from the TFPGA that originate from VHS-ADC cards. Clock and control signals are under the firmware direction.

**Testing:**
Boundary Scan.
Down load test pattern from TFPGA. Observe waveforms at SK19 & SK20.

## Reset

This is a High – Low- High, 140ms reset pulse generated by U7 on SchPg1. Reset will be issued on power up and on the depression of the push button SW1. Reset is directly connected to the TFPGA and its function is under firmware control.
It is not hard wired to reset any device on board TDRI.

**Testing:**
Boundary Scan.
Custom firmware.

## EEPROM and JTAG1

PL115, U62 (buffer), U61 (EEPROM), SW3, PL116, PL127-132 shown in SchPg8 makes up the TFPGA programming circuit.

**Programming U61 via PL115 JTAG connector:**
Open PL127, P129-PL132.
Close PL116, PL128 pin 2A-3A.
Connect JTAG plug to PL115.
Down load code to U61.
TFPGA can be programmed by pulsing CF under JTAG command or by pushing SW3.

**Programming U61 via Xport:**
Close PL127, P129-PL132.
Close PL116, PL128 pin 2A-1A.
Use Xport to down load code to U61.
TFPGA can be programmed by pulsing CF or XPROG under Xport command or by pushing SW3.

**Testing:**
Boundary Scan.
Custom Firmware.

**JTAG2**

PL126, U65 (buffer) and U1 (TFPGA) shown in SchPg8 makes up the TFPGA JTAG circuit. JTAG2 chain contains only the TFPGA. Connect JTAG plug to PL126 to commence testing.

**Testing:**

Boundary Scan.

**TFPGA**

Xilinx Virtex Π, XC2V1000-4FG456C shown in SchPg1 is the chosen TFPGA.
VREF pins of the TFPGA can be connected to 1.5V for a wider choice of signalling standards by closing PL5-PL44. All I/O should be compatible to +3.3V standards as defined in the Xilinx manual.
DCI of all banks are set at 51Ω.
Programming mode and pull up resistor enable can be selected by SW2.
U8 is an external temperature sensor added to monitor the substrate temperature of the TFPGA via Xport.
Pin List (To be added)

**Testing:**

Boundary Scan.
Custom Firmware.

**Power**

SChPg10 shows the power circuits. DC-DC and linear regulators are used derive the appropriate output voltages from the NIM crate power supply inputs.

3V3: Input to this DC-DC regulator is from +6V. Output 3.3V supplies Xilinx VCCO and the 3.3V required by all onboard digital ICs in general.

A3V3: Input to this DC-DC regulator is from the NIM +6V supply. Output 3.3V supplies Xilinx Auxiliary voltage only (i.e. clean 3.3V).

1V5: Input to this DC-DC regulator is from the NIM +6V supply. Output 1.5V supplies Xilinx Core voltage only.

AVCC: Input to this linear regulator is from the NIM +6V supply. Output 5.0V supplies the DAC analogue voltage only.

VEE: Input to this linear regulator is from the NIM -6V supply. Output -5.0V supplies the NECL circuits and the output pull down resistors.

VSS: Input to this linear regulator is from the NIM -6V supply. Output -2.0V supplies the single ended NECL input terminator resistors.

**Power Estimations:**
Regulators hanging from the NIM +6V supply may draw up to 8A Max and dissipate 48W max.
Regulators hanging from the NIM -6V supply may draw up to 3A Max and dissipate 18W max.
Estimated Max power dissipation of TDRI = 66W.

**Testing:**
Before powering up for the first time check for shorts at the inputs and outputs of the regulators using a multimeter.
Note Power to Ground DC resistance values for each power rail.

**LEDs**
SChPg 8 shows the LEDs. If the LED is 'On' the function described below is active. If function is described as 'Data' then the LED can be either 'On' or 'Off' barring a fault in the LED circuit.

| Name | Function |
|---|---|
| DS1 | Data (special) |
| DS2 Top | TFPGA Programming Done |
| DS2 Bot | TFPGA overheating |
| DS3 Top | A3V3 alive |
| DS3 Bot | VEE (-5V) alive |
| DS4 | Data (0) |
| DS5 | Data (1) |
| DS6 | Data (2) |
| DS7 | Data (3) |
| DS8 | Data (4) |
| DS9 Top | VSS (-2V) alive |
| DS9 Bot | AVCC (+5V) alive |

If DS1 to DS8 is 'Off' 3V3 may be at fault.