Overview of the Euroball Trigger System

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This document describes the Euroball Trigger System defined by Lazarus and Ender during 1989 as part of the Euroball Electronics specification, and later implemented in Eurogam and the Crystal Ball. Currently the system is in use for Euroball and EXOGAM.

The Euroball trigger system is designed to permit complex modes of operation of both the array itself and with external detectors. In order to achieve this flexibility, some local intelligence is necessary in each electronics signal processing channel, a so called Local Trigger (LT), which decides what to do in response to broadcast global trigger data from the Master Trigger card (MT).

A simple sequence of events would be as follows (see fig 1 on page 2):

1) Gamma rays detected in one or more Ge detectors by firing of CFD(s) in Ge electronics.

2) Electronics for each Ge detector drives a current sumbus for a pre-programmed length of time after an adjustable (time alignment) delay, such that all the pulses from the coincident gamma-rays are summed on the current sumbus. (typical pulse width 50ns, delay 100ns)

3) Master Trigger examines the sumbus and detects when fold is ≥ the programmed level, responding by generating a Fast Trigger pulse of a programmable width after a programmable delay. Master Trigger also starts a gate and delay timer to gate the Validation (2nd level trigger) logic later (ValGate).

4) All Local Triggers (in Ge electronics) started timers when their CFDs fired, and after a programmable time will sample the Fast Trigger pulse to see whether or not the channel is part of an event recognised by the master trigger. If not, then the channel aborts processing and waits for another gamma ray. Otherwise pulse peak detection and conversion continues.
The back edge of the FT pulse also stops a TAC in every channel which is started by the CFD. The FT is limited to the range 0-2μs from the CFD firing so as to optimise TAC resolution in the Ge electronics. It also allows a better time resolution for the FT sample points in Local Triggers for the same reason of restricted range.

5) When the Master Trigger's Validation gate pulse is generated, the Validation logic condition is checked (e.g. recoil detected or not) and a Validation pulse is generated if the condition is fulfilled. If there is no Validation logic condition to be checked then the Validation pulse is generated as soon as the ValGate input is generated. (The Validation pulse is limited to the range 2μs - 10μs after the CFD fires, these numbers being the limit of the FT pulse at the start and the end of shaping + conversion at the end. Validation may not be delayed longer than 10μs; slower signals must be correlated in software later.)

6) The Local Trigger's timing circuit makes a second check at the pre-programmed time when the Validation pulse is expected. If the Validation pulse exists when it is sampled then the event goes on to readout, but if Validation is not present when it is sampled then the channel aborts processing and waits for another gamma-ray.

7) The Validation pulse is also the signal to the readout mechanism that an event has been detected and so data must be read. So as to distinguish between multiple concurrent events, the trigger system tags each event with a 4 bit number during Validation. This number allows the readout system to select the event for which it requires data in a particular readout cycle. The use of a 4 bit code allows up to 16 concurrent events, and with a typical event processing time of 16μs this equates to an event rate of 1MHz and was considered to be adequate for any sensible experiment.

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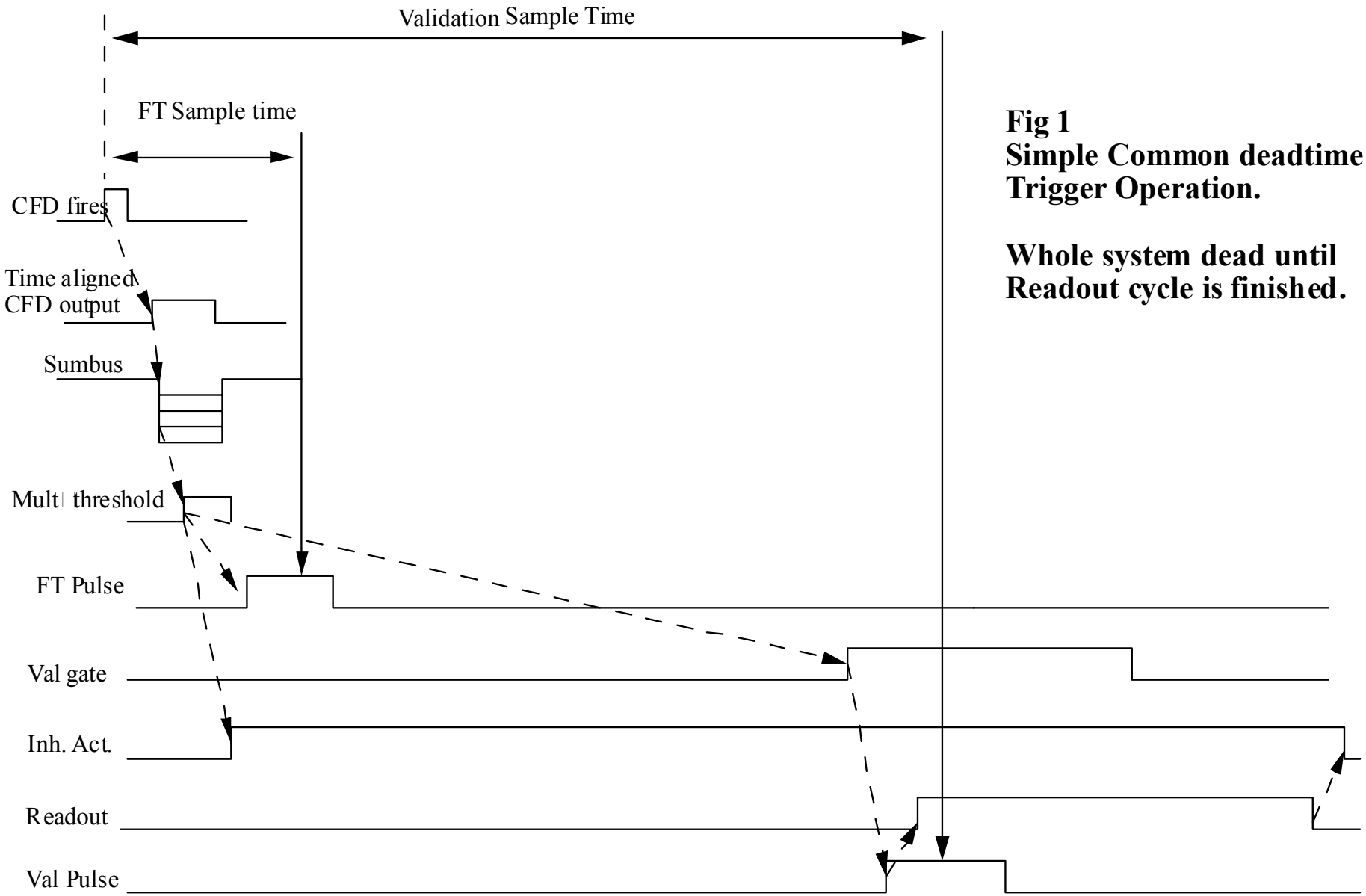

Fig 1
Simple Common deadtime Trigger Operation.

Whole system dead until Readout cycle is finished.

The preceding example is a simple one. Very complex triggers can be constructed and different modes of system operation supported using the same trigger architecture.

System Operation Methods:

1) Common dead time (all detectors dead until the end of readout)
2) Parallel operation (only detectors involved in the event are dead)
3) Pipelined operation (Pulse shaping and ADC conversion for the following event are permitted before completion of readout for present event.)
4) Parallel and pipelined.

Trigger types supported are:

1) Prompt coincidence
2) Delayed coincidence
3) Gamma only triggers
4) Particle only triggers
5) Particle-gamma triggers
6) Recoil-gamma triggers (prompt or delayed)
7) Just about anything else you can think of!

Normal Euroball III parallel operation is shown on the next page in fig 2.

The difference between the system operation modes is mainly in the length of time for which the Master Trigger asserts the Inhibit Action VXI line: for Common Dead time the system is inhibited by the MT from the time a Fast Trigger is generated until the end of readout. In parallel or pipelined systems the inhibit period is from the Fast Trigger for a programmable period, at least 0.5μs longer than the width of the Validation pulse, which is the shortest time to allow the unique identification of events by ensuring that the Validation pulses cannot overlap.

For parallel and pipelined modes the Local Triggers in active channels must generate and control their own local inhibits whilst they are busy (either on a per channel basis or a per-detector basis). In parallel mode the local inhibit covers the period from the CFD firing up to the end of readout of this channel's data (unless a missing Fast Trigger or a missing Validation indicates earlier that the event has been aborted). In pipelined mode the local inhibit lasts until the first processing stage (shaping) is free for another input. The time varies according to the shaping time constant. Clover card peaking time is about 4.5μs, and the shaping amplifier is busy for about 8 or 9μs. However, Cluster Ge cards use a 4μs time constant trapezoidal shaping. The sum of the peaking and flat top time is about 9μs and the shaping amplifiers are busy for over 20μs. So 11μs is available for ADC conversion (4.5μs) and card readout which means that pipelined mode gains nothing unless readout takes more than 7μs. Where readout is slow because many parameters are read, a limited form of pipelining could be envisaged where the channel is dead until the ADCs have converted and the data are stored in a local readout buffer.

The conclusion to be drawn from the previous paragraphs is that parallel operation has a more significant effect in improving system performance than pipelining. Pipelining brings little benefit because the shaping amplifier busy time in Cluster Ge cards limits system throughput, a trade-off introduced in EB4 in order to optimise Cluster detector energy resolution.

In parallel mode the absolute efficiency will no longer be constant when events overlap (because part of the system is already dead, effectively reducing the number of available detectors). It could, however, be argued that in the case of Cluster Ge cards these channels would be unavailable due to pileup anyway whether the system is in common deadtime or parallel mode. The pileup argument is not true for Clover channels where the amplifiers have shorter shaping times and so are busy for less than 10μs, but the channel will be dead for at least twice period this for parallel events including Cluster Ge cards.

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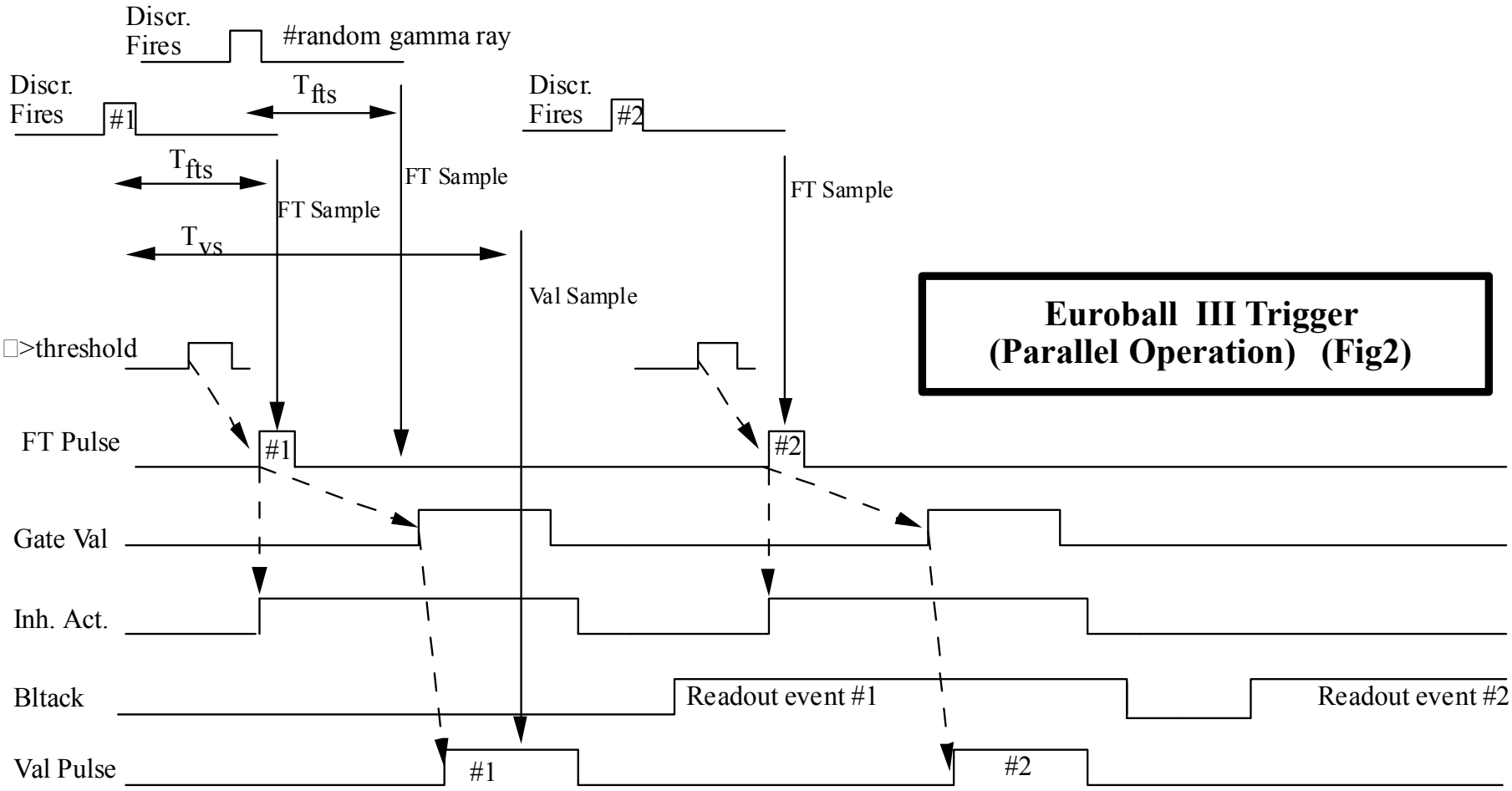
The local trigger in each channel starts timing when it detects a gamma ray (discr. fires). It contributes to a current sumbus for multiplicity which might or might not result in a Fast Trigger pulse depending on the number of other coincident channels. After a programmable time, T_{fs}, the local trigger checks for the existence of a FT pulse (usually clocks a D type flip flop). If there is no FT, the channel resets and waits for a good event. If FT exists the channel continues normal operation and later samples in the same way the Val pulse after a programmable time $T_{vs.}$ If the validation pulse exists then the event will be read out, but if there is no Val pulse at time T_{vs}, the channel resets without readout.



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The purpose of the MT is to recognise when an event has taken place and to inform the rest of the system. It records some information about the event itself such as the 32 bit event number which it has allocated, the maximum pulse height on the multiplicity sumbuses and the trigger type (only useful where multiple trigger conditions are OR'ed). The MT has 2 sources of information from which to recognise events: firstly the number of detectors which fired in coincidence (multiplicity) and secondly a set of 8 logic inputs on its front panel. As a result of these sources of information the MT, if it recognises a good event, will generate 2 trigger pulses: first the Fast Trigger Pulse (FT) and later the Validation Pulse (Val). The first of these, the FT, is used by the detector electronics as an indication that an event has occurred and as a global time reference. The Val is used by the detector electronics to confirm that, after further checks, the MT still considers this a good event and that readout will take place. The Val tells the STR8080 (Readout Controller) card to initiate readout and at the same time as the Val pulse the MT labels the event with an event number, the bottom 4 bits of which are broadcast over the VXI backplanes to the STR8080 and all the VXI detector electronics to tag the event. The event numbers are generated sequentially, so the STR8080 queues readout requests sequentially and detector electronics VXI cards can use FIFO memories to buffer labeled data because events will always be read in time order.

The user interacts with the MT using MIDAS software: there are no adjustments to be made on the card itself.

Front Panel Inputs:

Raw Ge sumbus (10 Lemo 00)	From every RM “Sum” output
Clean Ge sumbus (10 Lemo 00)	From every RM “AS1” output
BGO Sumbus (2 Lemo 00)	From every RM “AS2” output
User sumbus (2 Lemo 00)	From user’s electronics
Logic Inputs (8 Lemo 00)	From user’s electronics (signal type set from software) (Fast NIM, Slow NIM, ECL, TTL or user defined logic)
Note: all 8 logic inputs have their own independent programmable threshold	
14 way ribbon cable from RM	Contains various system control signals
Inhibit Request (1 Lemo 00)	Allows user’s electronics to pause Euroball by inhibiting the generation of triggers. Fast NIM logic.
Tref input (1 Lemo 00)	Time reference to qualify FT logic decision (Fast NIM)
TAC Stop (1 Lemo 00)	Stops MT's internal TAC (Fast NIM)
Val Out (1 Lemo 00)	The Validation pulse is provided here for user logic

Front Panel Outputs:

FT Pulse (12 Lemo 00)	Fast NIM logic. To RM SXin input (and user electronics)
Buffered sumbus (4 Lemo 00)	Each sumbus is buffered out for use by user logic (current)
Disc. Out (1 Lemo 00)	From discriminator applied to 1 of the 4 sumbuses (Fast NIM)
40 way ribbon cable to RM	Contains various system control signals including the Validation Pulse and Inhibit Action among others.

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Theory of Operation of the Master Trigger

The MT card contains a programmable logic array implemented in an integrated circuit called a Logic Cell Array (LCA). The FTV LCA recognises the FT condition(s) and the Validation condition(s). There is a library of programs for this LCA which covers nearly all experiments although it is possible to create a new program for esoteric experiments by arrangement. The operation of the card is governed by what happens within the FTV LCA. The LCA monitors the inputs (sumbus thresholds, logic inputs and system control inputs) and generates outputs as a result of what input conditions are detected.

A wide selection of inputs is available to the FTV LCA, some or all of which can be used in each decision. The LCA can monitor all 4 sumbuses, looking at between 1 and 4 different multiplicity threshold conditions on each sumbus (10 inputs in total, each programmable outside the LCAs in the range multiplicity ≥1 to 40). Additionally the FTV LCA can look at some or all of the 8 Logic inputs. All the sumbus thresholds and 4 of the logic inputs are available in time aligned form (after delay and stretch circuits). All 10 of the sumbus threshold decisions and all 8 logic decisions are also connected directly to the FTV LCA, making a total of 32 inputs to the LCA.

Outputs from the FTV LCA are firstly the signal that triggers the delay and stretch circuit for the FT pulse output, and secondly an 8 bit event type field which is sent to a pattern (or event type) register. A further 4 FT type bits are written to an external FIFO and read back into the FTV LCA again so as to enable different Validation conditions to be applied depending on the conditions causing the FT. The FIFO is only used in parallel mode. An Inhibit signal is also generated by the FTV LCA to prevent further events for either the period until the end of readout (common dead time) or the minimum inter-event gap (parallel/pipelined mode). Finally the FTV LCA starts a delay and stretch circuit which generates the gate signal (ValGate) for the validation decision logic. The gate is of fixed duration and occurs a fixed time after the FT pulse.

The simplest trigger is just to generate an FT when multiplicity on one of the RawGeSumbus thresholds is ≥N (N is set by a software slider independent of the LCA) and the Validation decision is always true (i.e. the Val Pulse delay and stretch circuit is triggered whenever the ValGate gate signal is received).

A more complex trigger would look for two different multiplicity levels on 2 different thresholds (e.g. RawGeThresh1 ≥ M and RawGeThresh2 ≥ N where M > N). In this case we would also use the trigger type bits, for example multiplicity M is type 1 and multiplicity N is type 2. On seeing the ValGate gate signal, the validation logic would examine the trigger type bits, and if it saw type 1 then it would generate a Validation pulse anyway, but if it saw type 2 then it would require that one of the Logic inputs was true during the ValGate gate period. This is a typical RMS experimental set-up (or any other ancillary detector which generates a logic signal between 2μs and 10μs after the initial gamma ray emission). If both type 1 and type 2 conditions were met, so both were true, then the user would choose whether the FTV LCA required that the type 2 logic input were present before making a validation or not. Normally and OR of the two possibilities is used, so type 1 normally takes precedence (i.e. no logic condition for validation; existence of the ValGate signal alone is sufficient).

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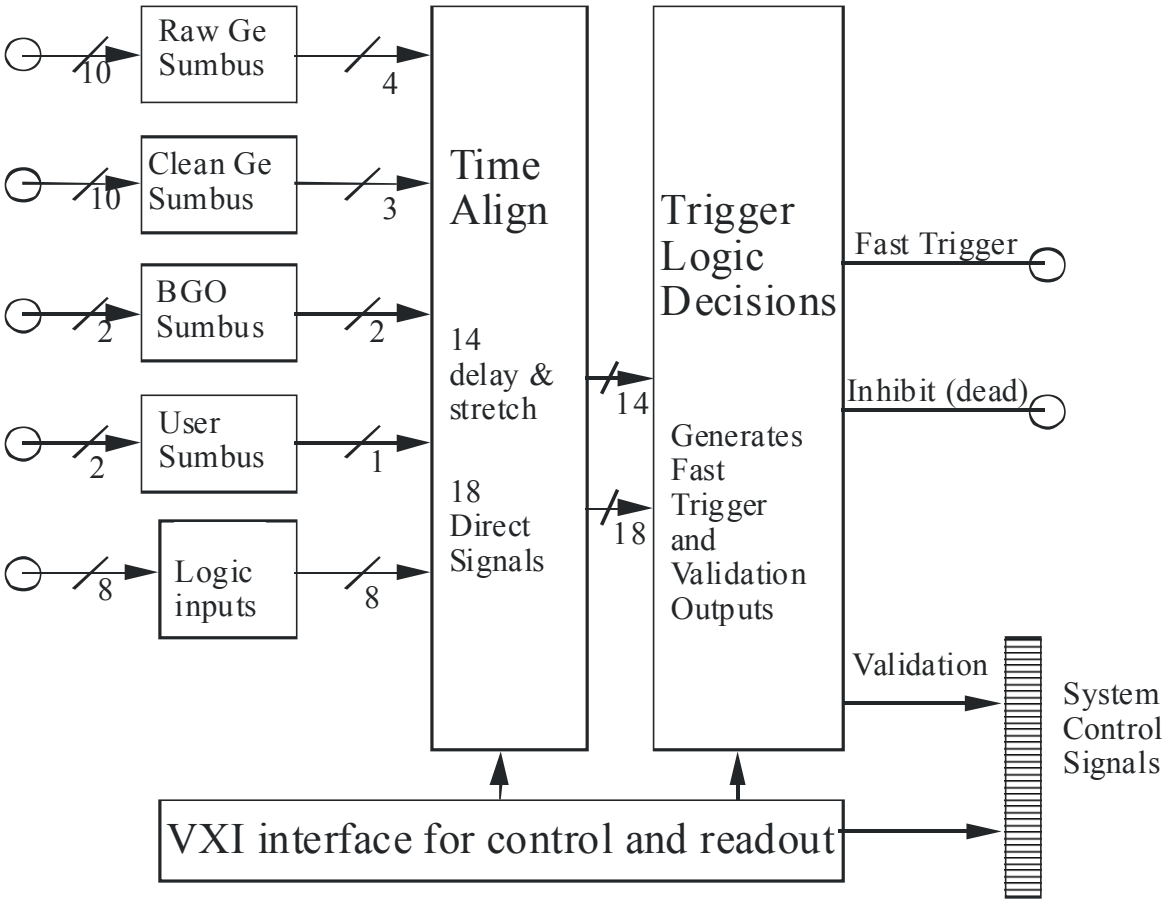

Simplified Block diagram of the Euroball/Exogam Master Trigger card

(Scalers, TAC and Sumbus peak sensing ADCs not shown)

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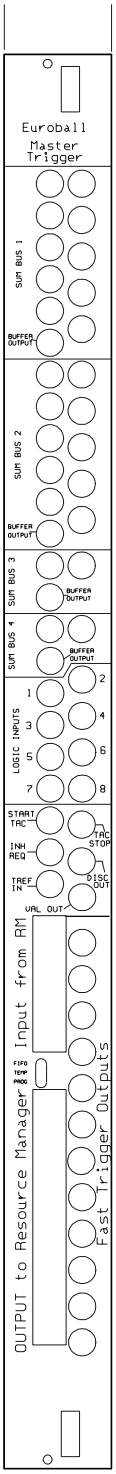

Front Panel of Master Trigger Card

Specification of Euroball Trigger Card

The Trigger card is a D sized VXI card that examines a programmable set of its input signals using a Xilinx LCA FPGA and controls nuclear physics experiments based on those inputs.

Inputs:
4 analogue sumbus inputs connected to 4,3,2 and 1 leading edge discriminators for ≥ fold decisions using up to 4 different folds for each sumbus. LCA sees inputs both direct from discriminators, and also after programmable time alignment circuits (delay 0-2μs, width 0-2μs).

Total 20 inputs to trigger decision FPGA.

8 Front panel logic inputs with a common programmable threshold (fast NIM, ecl, TTL, slow NIM). 4 of these inputs are also connected to time alignment circuits (delay 0-12μs, width 0-12μs) making a total of 12 inputs to the trigger decision FPGA.

1 Front panel Time Reference signal (fast NIM) (used for very accurate Fast Trigger timing).

System input signals are connected via a14 way differential ecl cable. These are Readout, Inhibit Request and Coding. Inhibit Request may also be driven via a fast NIM input.

Stop and Start inputs for the trigger's TAC are provided.

Outputs:
Fast Trigger: (12 Fast NIM Lemo 00 outputs)

System output signals are connected via a 40 way differential ecl cable. These are: Validation, Synch for Test Pulsers, Event Number (bits 0-3), VXI GO, Clear, Event Reject, Inhibit Action and Transfer Scalers to shadow registers.

Fold discriminator logic output (1) for use by ancillary detectors.

Scalers:
The Trigger card contains 8 scalers (32 bit) to count Fast Triggers, Validations, Readout cycles, Trigger Requests and a user selected signal from the trigger decision FPGA.

TAC:
A 0-2μs TAC is provided with Stop and Start software selectable to come from either the front panel or from one of the sumbus fold discriminators.

Readout and VME Interface
The VXI backplane interface for readout and control uses the Euroball standard GIR.
Data words are defined by the configurable FPGAs. For Euroball they will be some or all of the trigger type, the event number the TAC and the sumbus fold levels coded in ADCs.
For EXOGAM a timer counter could be added in the fpga's if required (max. rate 25MHz).

System Control
The system event number is generated in the trigger card and distributed from it during readout. The LS 4 bits are also broadcast to maintain system synchronisation.

The Fast Trigger, validation, event rejection and flow control are all generated by the trigger card and the register where the VXI GO/STOP bit is generated is also located in the trigger card.

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